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Implementation of Multilevel Inverter-Fed Induction Motor Drive

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Abstract

This paper presents the simulation and implementation of multilevel inverter fed induction motor drive. The output harmonic content is reduced by using multilevel inverter. In symmetrical circuit, the voltage and power increase with the increase in the number of levels of inverter. The switching angle for the pulse is selected in such way to reduce the harmonic distortion. This drive system has advantages like reduced total harmonic distortion and higher torque. The model of the multilevel inverter system is developed with SVM strategy to control the induction motor. The experimental results coincide with simulation results.

Introduction

DC motors have been used during the last century in industries for variable speed control applications, because its flux and torque can be controlled easily changing the field and armature currents respectively. Furthermore, four quadrant operation of induction motor was also achieved. Induction motor is popularly used in industries due to ruggedness and robustness. The induction motors were mainly used for essentially constant speed applications because of the unavailability of the variable-frequency voltage supply. The advancement of power electronics has made it possible to vary the frequency of the voltage. Thus, it has extended the use of induction motor in variable speed drive applications. The concept of multilevel inverter control has opened a new possibility that induction motors can be controlled to achieve dynamic performance equally as that of DC motors.

It has been found that the dynamic model equations developed on a rotat-

ing reference frame is a better way to describe the characteristics of induction motor. Variable speed induction motor drives are widely spread in electromechanical systems for a large spectrum of industrial applications. When high dynamic performance and high precision control in a wide speed range are required, vector control based induction motor drive can be used with speed sensor (D. Hadiouche, H. Razik, and A. Rezzoug, 2000). On the other hand, for medium and low performance applications, sensor-less control of induction motor is becoming an industrial standard. The recent advancement in power electronics has been initiated to improve the level of inverter rather than increasing the filter size. Using multilevel inverters, it is better to reduce the harmonics. In this paper, space vector modulation technique that uses to reduce the harmonics. For redundant switching, a space vector modulation is required due to vector selection in dq stationary reference frame. The space vector modulation technique is used for multilevel inverter system. However, space vector modulation has more advantages due to low harmonic production (K. Yamanaka et al., 2002).

The performance of the multilevel inverter is better than a classical inverter. The total harmonic distortion of the classical inverter is very high. In other words the total harmonic distortion for multilevel inverter is low. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. The voltage across the switches is only half of the DC bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device. A normal neutral point potential stabilization technique using the information of output current polarity is proposed by K. Yamanaka et al. (2002). The neutral point potential balancing algorithm for three level neutral point clamped inverters using analytically injected zero sequence voltage is developed by Q. Song (2003). Modulation schemes to eliminate common mode voltage in multilevel inverter topology is suggested by H. Zhang (2000). A generalized multilevel inverter topology with self voltage balancing is suggested by F Zeng Peng (2001). Survey of topologies, control and applications of multilevel inverters was done by J. Rodriguez (2002). Digital modulation technique for dual three phase a.c machines has been presented by R Bojoi (2002). Space vector PWM technique for dual three phase a.c machine and its DSP implementation has been presented by Hadiouche (2006). Practical medium voltage converter topologies for high power applications is presented by Steimer (2001). In the above mentioned literature, implementation of multilevel inverter using embedded controller is not presented. The present work deals with implementation of embedded controlled multilevel inverter fed induction motor drive. The details of simulation, control circuit and hardware are presented in this paper.

Voltage Vectors

Voltage vectors are required to view the voltages in the q-d stationary reference frame. The resulting vector plot contains information from all three phases and displays redundant switching states. The plot is particularly useful for comprehending the higher number of switching states. In addition, some mathematical relationships and derivations can be readily obtained from the vector plot. The vector diagram has also been used to formulate multilevel modulation. However, it will be shown later that this is more readily accomplished in the time domain. The inverter voltages can be expressed in the arbitrary *q*-*d* reference frame by

$$\begin{bmatrix} v_{qv} \\ v_{dv} \\ v_{ov} \\ v_{on} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{og} \\ v_{bg} \\ v_{cg} \end{bmatrix}, \quad (1)$$

The *q*-*d* stationary voltages can be expressed in terms of the switching states by

$$v_{qn}^{s} = \frac{v_{dc}}{3(n-1)} (2s_{a} - s_{b} - s_{c})$$
 (2)

$$v_{dn}^{s} = \frac{v_{dc}}{\sqrt{3}(n-1)} (s_{c} - s_{b})$$
(3)

The vector plot created by graphing the voltage vector defined by

$$\nu_{sw} = \nu_{qn}^s - j\nu_{dn}^s \tag{4}$$

for all possible switching states. Figure 1 indicates the vector plot for the three level inverter. Therein, each vector v_{sw} is denoted with a unique number. For the general *n* level inverter vector number related to the switching state can be represented as

$$sw = n^2 s_a + n s_b + s_c \tag{5}$$

Several vectors can be formed based on number of switching states. This switching state redundancy occurs since the common-mode component of the switching states is not included in the two-dimensional voltage vector plot. For the general *n*-level three-phase inverter, there are

$$\mathbf{n}_{\rm out} = \mathbf{n}^3 \tag{6}$$

switching states and

$$n_{vec} = 3n (n-1) + 1$$
(7)

Redundant switching states

The redundant switching states seen in Figure 1 provide some flexibilities in the multilevel systems and will be used to achieve control objectives in later sections. It is helpful to define some basic redundant state relationships.

The number of redundant states for a particular switching state set can be calculated by

$$n_{RSS} = n - (s_{max} - s_{min})$$
(8)

where s_{max} and s_{min} are the maximum and minimum of the switching state set or

$$\mathbf{s}_{\max} = \max\left(\mathbf{s}_{a}, \mathbf{s}_{b}, \mathbf{s}_{c}\right) \tag{9}$$

$$s_{\min} = \min(s_a, s_b, s_c) \tag{10}$$

Since this redundancy involves all three phases, it is referred to as joint-phase redundancy. It will be shown in later sections that some multilevel topologies have redundancy within each phase. This per-phase redundancy can be used or combined with joint-phase redundancy to achieve certain control objectives such as capacitor voltage balancing.

Space Vector Modulation

SVM is based on vector selection in the q-d stationary reference frame. Consider the commanded voltage vector defined for a three-level system, the commanded vector is plotted along with the vectors obtainable by the inverter in Figure 1. The desired vector v^{S^*}

 $v_{qds}^{S^*}$ is shown at some point in time, but it will follow the circular path if a three-phase set of voltages are required on the load. The circular path shown in the Figure.1, may be arbitrary. The first step in the SVM scheme is to identify the three nearest vectors.

Figure 1. Voltage vector plot v6 v15 v24 v7 v3,16 v12,15 v21 v8 v4,17 v0,13,26 v9,22 v18 Vqs v5 v1,4 v10,33 v19 v11 v20

In this example, they are v_{52} , v_{56} , and the redundant vectors v_{36} and v_{57} . The next step is to determine the amount of time that must be spent at each vector in order for the average voltage to be equal to the commanded voltage. It can be done using some simple mathematical relationships. In particular, the vectors and their corresponding times are related by

$$\nu_{35},_{46} T_{35};_{46} + \nu_{41}, T_{41} \cdot + \nu_{45}, T_{45} = \nu_{qds}^{s^*} T_{sw}$$
(11)

where T_{sw} is the switching time of the PWM control which is the total time spent at each vector or

$$T_{sw} = T_{36,57} + T_{52} + T_{56}$$
(12)

Based on (11) and (12), the amount of time for each voltage vector can be computed by solving the inverse problem

$$\begin{bmatrix} \operatorname{Rev}_{3_{657}} & \operatorname{Rev}_{52} & \operatorname{Rev}_{56} \\ \operatorname{Im}_{v_{3_{657}}} & \operatorname{Im}_{v_{52}} & \operatorname{Im}_{v_{56}} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} T_{3_{657}} \\ T_{52} \\ T_{56} \end{bmatrix} = \begin{bmatrix} \operatorname{Rev}_{qds}^{s^*} \\ \operatorname{Im}_{v_{qds}}^{s^*} \\ T_{sw} \end{bmatrix}$$
(13)

The final step in the SVM scheme is to determine a sequence of switching for the Voltage vectors and the corresponding output voltage (Hadiouche .D,. Baghli .L, Rezzoug, A. 2006).

Multilevel inverter fed induction motor

AC input is rectified using a diode rectifier. It is filtered using a capacitor filter. DC is applied to the multilevel inverter. The output of the inverter is fed to the induction motor. This system is simulated using Matlab Simulink. The Simulink model for multilevel inverter fed system is depicted in Figure 2. Input pulses to the MOSFETs are generated by the sources V_1 to V_6 . The phase voltage and line to line voltages are measured by the scopes connected at the output. The scope is connected to measure parameters like voltage, rotor speed and torque. The pulses are generated using SVM method. The speed loop ensures that the actual speed of the motor is equal to set speed. The current

loop provides protection for the devices in the inverter.

Simulation Results

Simulink is selected since the simpowersystem module is useful for simulating drive systems. The circuit model of multilevel inverter fed induction motor system is given in Figure 2. An uncontrolled rectifier converts AC in to fixed DC. DC is converted in to AC using three phase inverter. Induction motor block available in simulink is used for simulation studies. Scope 1 is used for displaying these voltages. Scope 3 is used for displaying the currents. The three phase voltage waveforms are indicated in Figure 3. The three phase current waveforms are represented in Figure 4. The currents lag the respective voltages since induction motor operates at lagging power factor.

Experimental Results

After the simulation studies, a microcontroller based multilevel inverter fed induction motor system is fabricated and tested. The control circuit is given in Figure 5. The top view of the hardware is depicted in Figure 6. The oscillogram of line voltage is given in Figure 7. The oscillogram of phase voltage is depicted in Figure 8. The Atmel microcontroller 89C2051 is used to generate the pulses. Port 1 of the microcontroller is used for generating the gate pulses. Timer 0 is used for producing the delay required for the duration T_{ON} and T_{OFF} . The microcontroller operates at a clock frequency of 12 MHZ. The pulses produced by the microcontroller are amplified using the driver IC IR 2110. Three driver ICs are used to amplify the gate pulses.





Figure 3. Three phase voltage waveforms



The regulators 7812 and 7805 in the control circuit give the DC supply required by the driver and microcontroller chips respectively. The driver chip amplifies 5V pulse to 10V level.

Conclusion

Microcontroller based multilevel inverter fed induction motor drive is simulated using Matlab Simulink and the hardware is implemented on two prototype boards. The multilevel inverter output has reduced harmonics. This reduces the heat generated in the stator winding

of the induction motor. The torque of the motor is improved due to the elimination of the fifth harmonic, which produces negative torque. A Microcontroller based gating circuit generates the pulses required by the inverter. The induction motor drive system is successfully fabricated and tested. The applied research demonstrated that simulation and experimental results shown in Figures. 3 and 8 are consistent. The hardware system used in the present work has obvious advantage of using single phase supply. This drive can be used for variable speed applications like conveyors, rolling mills, printing machines.

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Figure 5. Microcontroller based control circuit



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Figure 7. Oscillogram of line voltage



Time(sec)

Figure 8. Oscillogram of phase voltage



Voltage (V) 40V/div

Time (sec)

